TC2117

800 mA Fixed Low Dropout Positive Regulator

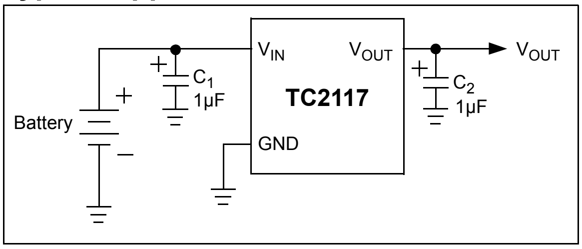
Features

- Fixed Output Voltages: 1.8V, 2.5V, 3.0V, 3.3V
- Very Low Dropout Voltage
- Rated 800 mA Output Current
- High Output Voltage Accuracy
- Standard or Custom Output Voltages
- Overcurrent and Overtemperature Protection
- Space Saving SOT-223 Package

Applications

- 5V to 3.3V Linear Regulator
- Portable Computers
- Instrumentation
- Battery Operated Systems
- Linear Post-Regulator for SMPS
- Core Voltage Supply for FPGAs, PLDs, CPUs, DSPs

Typical Application

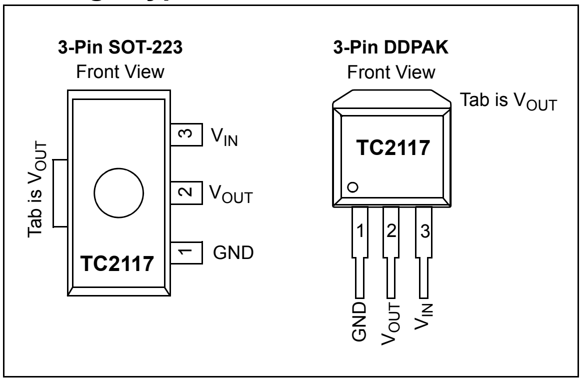


General Description

The TC2117 is a fixed, high accuracy (typically ±0.5%) CMOS low dropout regulator. Designed specifically for battery operated systems, the TC2117's CMOS construction eliminates wasted ground current, significantly extending battery life. Total supply current is typically 80 µA at full load (20 to 60 times lower than in bipolar regulators).

TC2117 key features include ultra low noise, very low dropout voltage (typically 450 mV at full load), and fast response to step changes in load. The TC2117 incorporates both overtemperature and overcurrent protection. The TC2117 is stable with an output capacitor of only 1µF and has a maximum output current of 800 mA. This device is available in 3-Pin SOT-223, and 3-Pin DDPAK packages.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input Voltage 6.5V
Output Voltage.................... (V_{SS} – 0.3) to (V_{IN} + 0.3V)
Power Dissipation................Internally Limited **(Note 7)**
Maximum Voltage on Any Pin ....V_{IN} +0.3V to -0.3V
Operating Temperature ....-40°C < T_J < +125°C
Storage temperature ....-65°C to +150°C

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1.5V$, **(Note 1)**, I_L = 100 µA, C_L = 3.3 µF, T_A = +25°C.
Boldface type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**6.0**	V	**Note 2**
Maximum Output Current	I_{OUTMAX}	**800**	—	—	mA	
Output Voltage	V_{OUT}	**V_R – 2.5%**	V_R ± 0.5%	**V_R + 2.5%**	V	$V_R \geq 2.5V$
		V_R – 2%	V_R ± 0.5%	**V_R + 3%**		V_R = 1.8V
V_{OUT} Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	—	40	—	ppm/°C	**Note 3**
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	—	0.007	**0.35**	%	$(V_R + 1V) \leq V_{IN} \leq 6V$
Load Regulation **(Note 4)**	$\Delta V_{OUT}/V_{OUT}$	**-0.01**	0.002	0	%/mA	I_L = 0.1 mA to I_{OUTMAX}
Dropout Voltage **(Note 5)**	$V_{IN}–V_{OUT}$	—	20	**30**	mV	$V_R \geq 2.5V$, I_L = 100 µA
		—	50	**160**		I_L = 100 mA
		—	150	**480**		I_L = 300 mA
		—	260	**800**		I_L = 500 mA
		—	450	**1300**		I_L = 800 mA
		—	1000	**1200**		V_R = 1.8V, I_L = 500 mA
		—	1200	**1400**		I_L = 800 mA
Supply Current	I_{DD}	—	80	**130**	µA	$\overline{SHDN} = V_{IH}$, I_L = 0
Power Supply Rejection Ratio	PSRR	—	55	—	db	F ≤ 1 kHz
Output Short Circuit Current	I_{OUTSC}	—	1200	—	mA	V_{OUT} = 0V
Thermal Regulation	$\Delta V_{OUT}/\Delta P_D$	—	0.04	—	V/W	**Note 6**
Output Noise	eN	—	300	—	$nV/\sqrt{Hz}$	I_L = 100 mA, F = 10 kHz

Note 1: V_R is the regulator output voltage setting.

2: The minimum V_{IN} has to justify the conditions: $V_{IN} \geq V_R + V_{DROPOUT}$ and $V_{IN} \geq 2.7V$ for I_L = 0.1 mA to I_{OUTMAX}.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) - 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value measured at a 1.5V differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for T = 10 ms.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 4.2 "Thermal Considerations"** for more details.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1.5V$, $I_L = 100\ \mu A$, $C_L = 3.3\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	**(Note 1)**
Operating Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 3L-SOT-223	θ_{JA}	—	59	—	°C/W	
Thermal Resistance, 3L-DDPAK	θ_{JA}	—	71	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed Maximum Junction Temperature (+125°C).

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

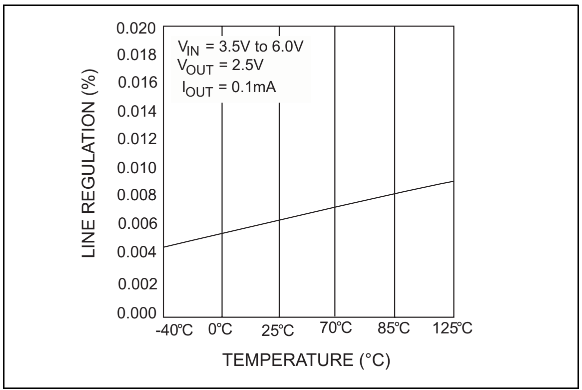


FIGURE 2-1: *Line Regulation vs. Temperature.*

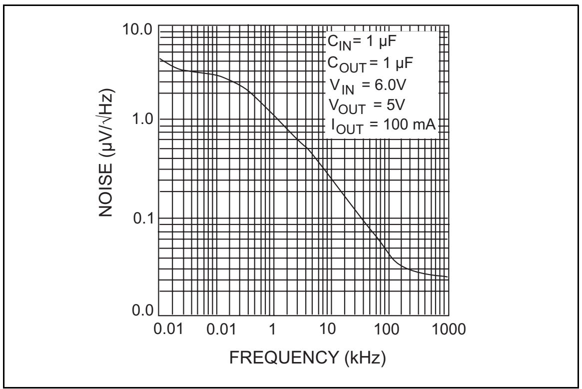


FIGURE 2-2: *Output Noise vs. Frequency.*

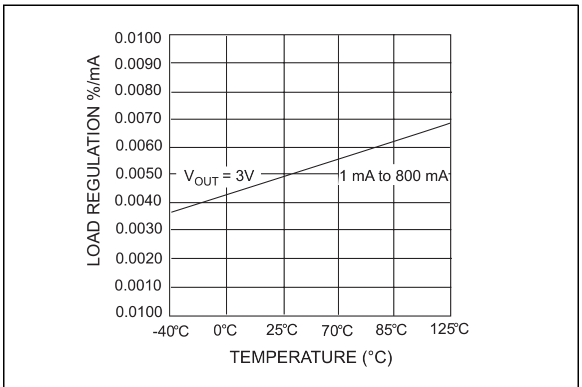


FIGURE 2-3: *Load Regulation vs. Temperature.*

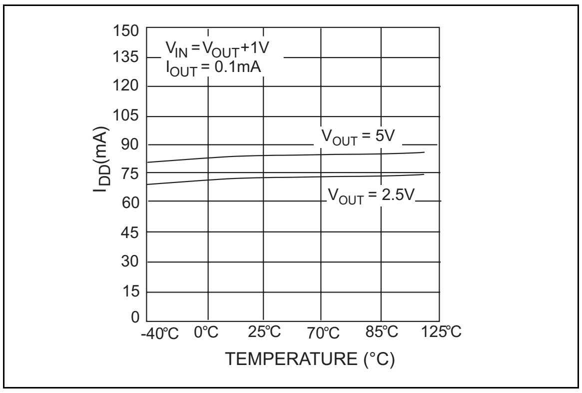


FIGURE 2-4: *I_{DD} vs. Temperature.*

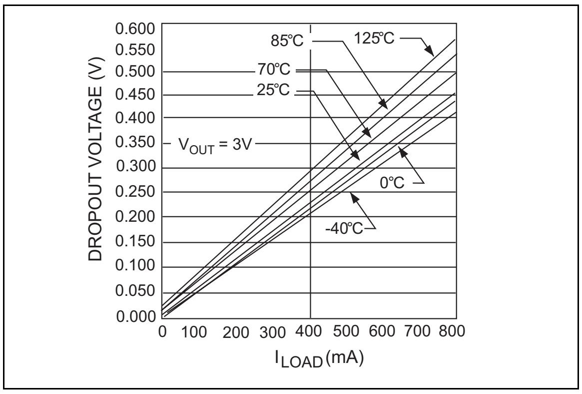


FIGURE 2-5: *Dropout Voltage vs. I_{LOAD}.*

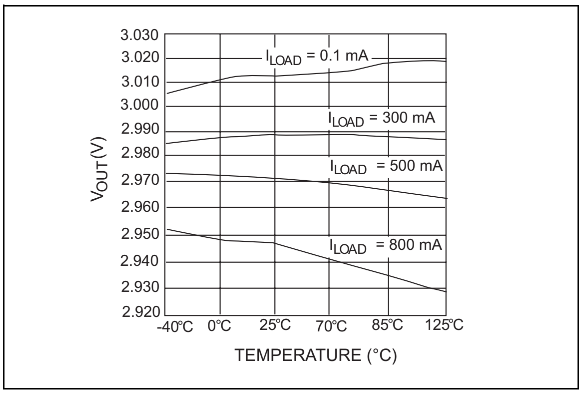


FIGURE 2-6: *3.0V V_{OUT} vs.Temperature.*

Typical Performance Curves (Continued)

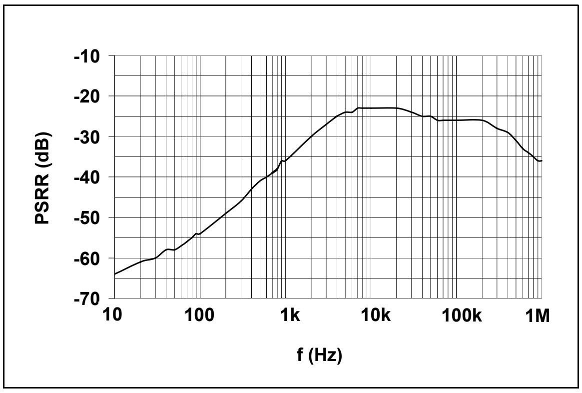


FIGURE 2-7: *Power Supply Rejection Ratio.*

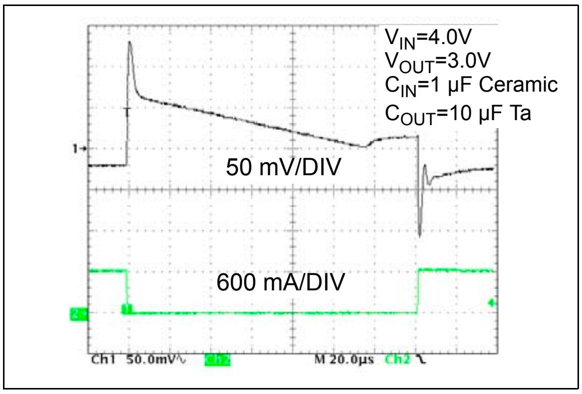


FIGURE 2-8: *Load Step Response.*

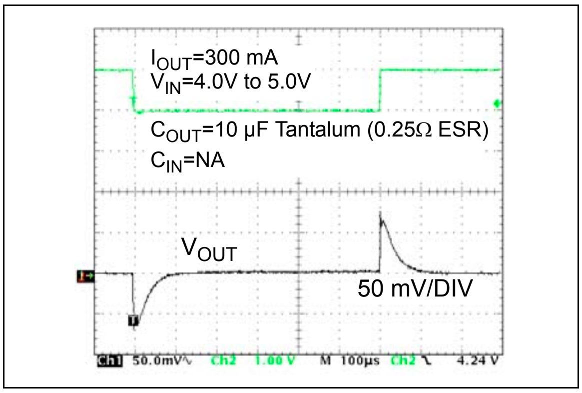


FIGURE 2-9: *Line Step Response*

3.0 PIN DESCRIPTIONS

The descriptions for the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. (3-Pin SOT-223) (3-Pin DDPAK)	Symbol	Description
1	GND	Ground Terminal.
2	V_{OUT}	Regulated output voltage.
3	V_{IN}	Unregulated Supply input.

3.1 Ground (GND)

Ground terminal.

3.2 Regulated Output Voltage (V_{OUT})

Regulated voltage output.

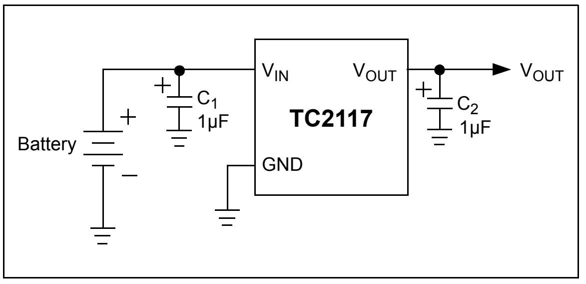
3.3 Unregulated Supply (V_{IN})

Unregulated supply input

4.0 DETAILED DESCRIPTION

The TC2117 is a precision, positive output LDO. Unlike bipolar regulators, the TC2117 supply current does not increase proportionally with load current. In addition, V_{OUT} remains stable and within regulation over the entire 0 mA to 800 mA operating load range.

FIGURE 4-1: TYPICAL APPLICATION CIRCUIT



4.1 Output Capacitor

A 1 µF (min) capacitor from V_{OUT} to ground is required. The output capacitor should have an effective series resistance of 0.2Ω to 10Ω. A 1 µF capacitor should be connected from V_{IN} to GND if there is more than 10 inches of wire between the regulator and the AC filter capacitor, or if a battery is used as the power source. Aluminum electrolytic or tantalum capacitor types can be used. (Since many aluminum electrolytic capacitors freeze at approximately -30°C, solid tantalums are recommended for applications operating below -25°C.) When operating from sources other than batteries, supply noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

4.2 Thermal Considerations

4.2.1 THERMAL SHUTDOWN

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

4.2.2 POWER DISSIPATION

The amount of power the regulator dissipates is primarily a function of input and output voltage, and output current. The following equation is used to calculate worst case actual power dissipation:

EQUATION 4-1:

$$P_D = (V_{INMAX} - V_{OUTMIN}) I_{LOADMAX}$$

Where:

P_D = Worst-case actual power dissipation
V_{INMAX} = Maximum voltage on V_{IN}
V_{OUTMIN} = Minimum regulator output voltage
$I_{LOADMAX}$ = Maximum output (load) current

The maximum *allowable* power dissipation (Equation 4-2) is a function of the maximum ambient temperature (T_{AMAX}), the maximum allowable die temperature (+125°C) and the thermal resistance from junction-to-air (θ_{JA}).

EQUATION 4-2:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

Where all terms are previously defined.

Table 4-1 shows various values of θ_{JA} for the TC2117 mounted on a 1/16 inch, 2-layer PCB with 1 oz. copper foil.

TABLE 4-1: THERMAL RESISTANCE GUIDELINES FOR TC2117 IN 3-PIN SOT-223 PACKAGE

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance
2500 sq mm	2500 sq mm	2500 sq mm	45°C/W
1000 sq mm	2500 sq mm	2500 sq mm	45°C/W
225 sq mm	2500 sq mm	2500 sq mm	53°C/W
100 sq mm	2500 sq mm	2500 sq mm	59°C/W
1000 sq mm	1000 sq mm	1000 sq mm	52°C/W
1000 sq mm	0 sq mm	1000 sq mm	55°C/W

* Tab of device attached to topside copper.

TABLE 4-2: THERMAL RESISTANCE GUIDELINES FOR TC2117 IN 3-PIN DDPAK PACKAGE

Copper Area (Topside)*	Copper Area (Backside)	Board Area	Thermal Resistance (θ_{JA})
2500 sq mm	2500 sq mm	2500 sq mm	25°C/W
1000 sq mm	2500 sq mm	2500 sq mm	27°C/W
125 sq mm	2500 sq mm	2500 sq mm	35°C/W

*Tab of device attached to topside copper.

Equation 4-1 can be used in conjunction with Equation 4-2 to ensure regulator thermal operation is within limits. For example:

Given:

V_{INMAX} = 5.0V ± 5%

V_{OUTMIN} = 3.3V ± 0.5%

$I_{LOADMAX}$ = 400 mA

T_{JMAX} = 125°C

T_{AMAX} = 55°C

θ_{JA} = 59°C/W (SOT-223)

Find: 1. Actual power dissipation

2. Maximum allowable dissipation

Actual power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN})I_{LOADMAX}$$

$$= [(5.0 \text{ x } 1.05) - (3.3 \text{ x } .995)]\ 400 \text{ x } 10^{-3}$$

$$= 786 \text{ mW}$$

Maximum allowable power dissipation:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

$$= \frac{(125 - 55)}{59}$$

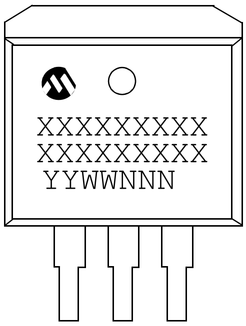
$$= 1.186\text{W}$$

In this example, the TC2117 dissipates a maximum of only 786 mW; below the allowable limit of 1.186W. In a similar manner, Equation 4-1 and Equation 4-2 can be used to calculate maximum current and/or input voltage limits.

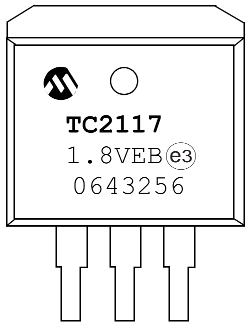
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

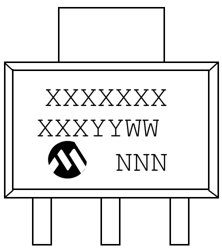
3-Lead DDPAK



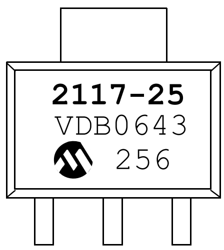
Example



3-Lead SOT-223



Example

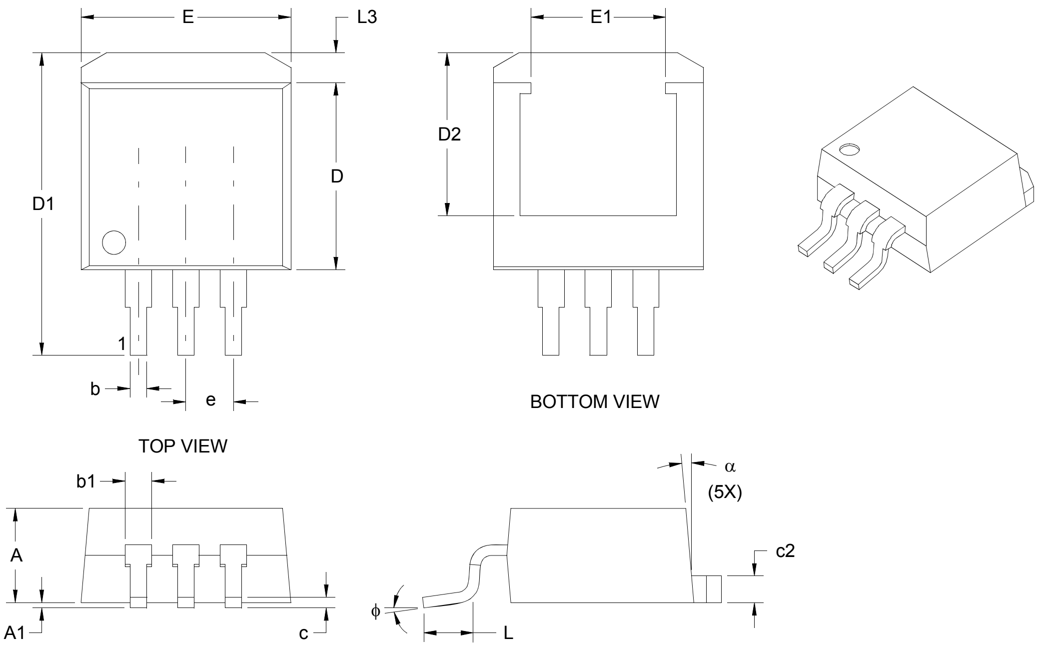


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead Plastic (EB) (DDPAK)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

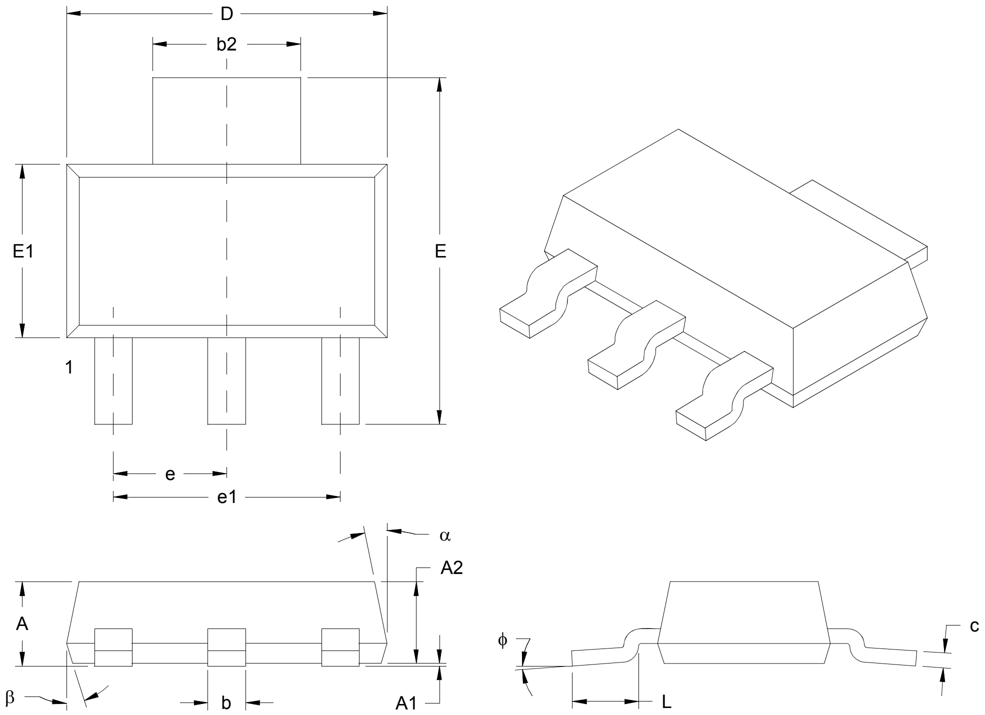


		Units	INCHES*			MILLIMETERS		
Dimension Limits			MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins				3			3	
Pitch		e	1.00 BSC			2.54 BSC		
Overall Height		A	.170	.177	.183	4.32	4.50	4.65
Standoff	§	A1	.000	.005	.010	0.00	0.13	0.25
Overall Width		E	.385	.398	.410	9.78	10.11	10.41
Exposed Pad Width		E1	.256 REF			6.50 REF		
Molded Package Length		D	.330	.350	.370	8.38	8.89	9.40
Overall Length		D1	.549	.577	.605	13.94	14.66	15.37
Exposed Pad Length		D2	.303 REF			7.70 REF		
Lead Thickness		c	.014	.020	.026	0.36	0.51	0.66
Pad Thickness		c2	.045	--	.055	1.14	--	1.40
Lower Lead Width		b	.026	.032	.037	0.66	0.81	0.94
Upper Lead Width		b1	.049	.050	.051	1.24	1.27	1.30
Foot Length		L	.068	--	.110	1.73	--	2.79
Pad Length		L3	.045	--	.067	1.14	--	1.70
Foot Angle		φ	--	--	8°	--	--	8°
Mold Draft Angle		α	3°	--	7°	3°	--	7°

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
BSC: Basic Dimension. Theoretically, exact value shown without tolerances.
See ASME Y14.5M
REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M
JEDEC equivalent: TO-252
Drawing No. C04-011
Revised 07-19-05

3-Lead Plastic Small Outline Transistor (DB) (SOT-223)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	e	.091 BSC			2.30 BSC		
Outside lead pitch (basic)	e1	.181 BSC			4.60 BSC		
Overall Height	A	–	–	.071	–	–	1.80
Standoff	A1	.001	–	.004	0.02	–	0.10
Molded Package Height	A2	.061	.063	.065	1.55	1.60	1.65
Overall Width	E	.264	.276	.287	6.70	7.00	7.30
Molded Package Width	E1	.130	.138	.146	3.30	3.50	3.70
Overall Length	D	.248	.256	.264	6.30	6.50	6.70
Lead Thickness	c	.009	.012	.014	0.23	0.30	0.35
Lead Width	b	.026	.030	.033	0.65	0.76	0.85
Tab Lead Width	b2	.114	.118	.124	2.90	3.00	3.15
Foot Length	L	.035	–	–	0.90	–	–
Lead Angle	φ	0°	–	10°	–	0.37	10°
Mold Draft Angle, Top	α	10°	–	16°	10°	–	16°
Mold Draft Angle, Bottom	β	10°	–	16°	10°	–	16°

* Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

JEDEC Equivalent TO-261 AA

Drawing No. C04-032

Revised 09-13-05

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (October 2006)

- **Section 1.0 "Electrical Characteristics"**: Changed dropout voltage voltage typical value for I_L = 500 mA from 700 to 1000 and maximum value from 1000 to 1200 for. Changed typical value for I_L = 800 mA from 890 to 1200
- **Section 5.0 "Packaging information"**: Added package marking information and package outline drawings
- Added disclaimer to package outline drawings.
- Added Appendix A Revision History

Revision B (May 2002)

- Not Documented

Revision A (May 2001)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X.XX	XX	XX
Device	Voltage Option	Package	Tape and Reel

Device	TC2117		Fixed Output CMOS LDO Positive Regulator
Voltage Option:*	1.8V	=	1.8V
	2.5V	=	2.5V
	3.0V	=	3.0V
	3.3V	=	3.3V
	* Other output voltages are available. Please contact your local Microchip sales office for details.		
Package	DB	=	Plastic (SOT-223), 3-lead
	DBTR	=	Plastic (SOT-223), 3-lead, Tape and Reel
	EB	=	Plastic Transistor Outline (DDPAK), 3-Lead
	EBTR	=	Plastic Transistor Outline (DDPAK), 3-Lead, Tape and Reel

Examples:

a) TC2117-1.8VEBTR 1.8V LDO, DDPAK-3 pkg., Tape and Reel
b) TC2117-2.5VEBTR 2.5V LDO, DDPAK-3 pkg., Tape and Reel
c) TC2117-3.0VEBTR 3.0V LDO, DDPAK-3 pkg., Tape and Reel
d) TC2117-3.3VEBTR 3.3V LDO, DDPAK-3 pkg., Tape and Reel

a) TC2117-1.8VDB 1.8V LDO, SOT-223 pkg.
b) TC2117-1.8VDBTR 1.8V LDO, SOT-223 pkg., Tape and Reel
c) TC2117-2.5VDB 2.5V LDO, SOT-223 pkg.
d) TC2117-2.5VDBTR 2.5V LDO, SOT-223 pkg., Tape and Reel
e) TC2117-3.0VDB 3.0V LDO, SOT-223 pkg.
f) TC2117-3.0VDBTR 3.0V LDO, SOT-223 pkg., Tape and Reel
g) TC2117-3.3VDB 3.3V LDO, SOT-223 pkg.
h) TC2117-3.3VDBTR 3.3V LDO, SOT-223 pkg., Tape and Reel

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PIC® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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